Amendments to the Claims:

Please cancel claims 18-20 and 24-26.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Original) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a first controller which is connected to the first sense-amplifying unit and sets the output signal in response to a reset signal and an inverted signal of the reset signal;

a second controller which is connected to the second sense-amplifying unit and resets the complementary signal of the output signal in response to the reset signal and the inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, the first controller, and the second controller and responds to the clock signal.

2. (Original) The sense amplifier of claim 1, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

3. (Original) The sense amplifier of claim 1, wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the

first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a first output node from which the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the first controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the first controller.

4. (Original) The sense amplifier of claim 1, wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor

is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the second controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the second controller.

5. (Original) The sense amplifier of claim 1, wherein the first controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first sense-amplifying unit, and the ground voltage is applied to the gate of the second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source.

6. (Original) The sense amplifier of claim 1, wherein the second controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to

the second sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, and the power supply voltage is applied to the gate of the second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source.

7. (Original) The sense amplifier of claim 1, wherein the current source includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, the first controller, and the second controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

8. (Original) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a first controller which is connected to the first sense-amplifying unit and resets the output signal in response to a reset signal and an inverted signal of the reset signal;

a second controller which is connected to the second sense-amplifying unit and sets the complementary signal of the output signal in response to the reset signal and the inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-

amplifying unit, the first controller, and the second controller and responds to the clock signal.

9. (Original) The sense amplifier of claim 8, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

10. (Original) The sense amplifier of claim 8, wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a first output node from which the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the first controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the first controller.

11. (Original) The sense amplifier of claim 8, wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the second controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the second controller.

12. (Original) The sense amplifier of claim 8, wherein the first controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first sense-amplifying unit, and the power supply voltage is applied to the gate of the

second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source.

13. (Original) The sense amplifier of claim 8, wherein the second controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, and the ground voltage is applied to the gate of the second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source.

14. (Original) The sense amplifier of claim 8, wherein the current source includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, the first controller, and the second controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

15. (Currently Amended) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the

input signal in response to the clock signal and generates the complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a first output node from which the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

16. (Original) The sense amplifier of claim 15, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a first output node from which the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

22. (Original) The sense amplifier of claim 21, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Original) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal;

a first controller which is connected to the first sense-amplifying unit and sets the output signal in response to the reset signal and an inverted signal of the reset signal; and

a second controller which is connected to the second sense-amplifying unit and resets the complementary signal of the output signal in response to the reset signal and the inverted signal of the reset signal.

28. (Original) The sense amplifier of claim 27, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

29. (Original) The sense amplifier of claim 27, wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first NMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a first output node from which the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the

third PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the first controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the first controller.

30. (Original) The sense amplifier of claim 27, wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the second controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the second controller.

31. (Original) The sense amplifier of claim 27, wherein the first controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source; and

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the power supply voltage is applied to the source of the second NMOS transistor.

32. (Original) The sense amplifier of claim 27, wherein the second controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source; and

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the ground voltage is applied to the source of the second NMOS transistor.

33. (Original) The sense amplifier of claim 27, wherein the current source

includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, the first controller, and the second controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

34. (Original) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal;

a first controller which is connected to the first sense-amplifying unit and resets the output signal in response to the reset signal and an inverted signal of the reset signal; and

a second controller which is connected to the second sense-amplifying unit and sets the complementary signal of the output signal in response to the reset signal and the inverted signal of the reset signal.

35. (Original) The sense amplifier of claim 34, further comprising:
a first inverting buffer which buffers and inverts the output signal; and
a second inverting buffer which buffers and inverts the complementary signal of the output signal.

36. (Original) The sense amplifier of claim 34, wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first NMOS transistor, the reset signal is applied to the gate of the

second PMOS transistor, and the drain of the second PMOS transistor is connected to a first output node from which the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the first controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the first controller.

37. (Original) The sense amplifier of claim 34, wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the output signal output from the first sense-amplifying unit is applied to

the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the second controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the second controller.

38. (Original) The sense amplifier of claim 34, wherein the first controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source; and

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the ground voltage is applied to the source of the second NMOS transistor.

39. (Original) The sense amplifier of claim 34, wherein the second controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second sense-amplifying unit, the inverted signal of the reset signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the current source; and

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the power supply voltage is applied to the source of the second NMOS transistor.

40. (Original) The sense amplifier of claim 34, wherein the current source includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, the first controller, and the second controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

41. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal; wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a first output node from which the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the complementary signal of the output signal output from the second

sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

42. (Original) The sense amplifier of claim 41, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

43. (Canceled)

44. (Canceled)

45. (Canceled)

46. (Previously Presented) The sense amplifier of claim 41, further comprising a current source including an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the controller, the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

47. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal; wherein the first sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a first output node from which the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the complementary signal of the output signal output from the second sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the first output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the first output node, the complementary signal of the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to

the source of the first NMOS transistor, the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

48. (Original) The sense amplifier of claim 47, further comprising:

a first inverting buffer which buffers and inverts the output signal; and

a second inverting buffer which buffers and inverts the complementary signal of the output signal.

49. (Canceled)

50. (Canceled)

51. (Canceled)

52. (Previously Presented) The sense amplifier of claim 47, further comprising a current source including an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the controller, the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

53. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal; wherein the second

sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

54. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal; wherein the controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, the reset signal is applied to the gate of the first NMOS transistor, and the power supply voltage is applied to the source of the first NMOS transistor;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the ground voltage is applied to the source of the second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is commonly connected to the first sense-amplifying unit and the second sense-amplifying unit, and the inversion reset signal of the reset signal is applied to the gate of the third NMOS transistor.

55. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal, wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, and the clock signal is applied to the gate of the first PMOS transistor;

a second PMOS transistor, wherein the source of the second PMOS transistor is connected to the drain of the first PMOS transistor, the reset signal is applied to the gate of the

second PMOS transistor, and the drain of the second PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a third PMOS transistor, wherein the power supply voltage is applied to the source of the third PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the third PMOS transistor, and the drain of the third PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

56. (Previously Presented) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and a reset signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and the reset signal and generates a complementary signal of the output signal; and

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to the reset signal and an inverted signal of the reset signal; wherein the controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to

the first sense-amplifying unit, the reset signal is applied to the gate of the first NMOS transistor, and the ground voltage is applied to the source of the first NMOS transistor;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, the reset signal is applied to the gate of the second NMOS transistor, and the power supply voltage is applied to the source of the second NMOS transistor; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is commonly connected to the first sense-amplifying unit and the second sense-amplifying unit, and the inverted signal of the reset signal is applied to the gate of the third NMOS transistor.

57. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates the complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the output signal output from the first sense-amplifying unit is

applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

58. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates the complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, and the ground voltage is applied to the gate of the first NMOS transistor;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, and the power supply voltage is applied to the gate of the second NMOS transistor;

a third NMOS transistor, wherein the drain of the third NMOS transistor is commonly connected to the source of the first NMOS transistor and the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source; and

a fourth NMOS transistor, wherein the drain of the fourth NMOS transistor is commonly connected to the first sense-amplifying unit and the second sense-amplifying unit, the inversion reset signal is applied to the gate of the fourth NMOS transistor, and the source of the fourth NMOS transistor is connected to the current source.

59. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates the complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, sets the output signal and resets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the current source includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.

60. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the second sense-amplifying unit comprises:

a first PMOS transistor, wherein a power supply voltage is applied to the source of the first PMOS transistor, the clock signal is applied to the gate of the first PMOS transistor, and the drain of the first PMOS transistor is connected to a second output node from which the complementary signal of the output signal is output;

a second PMOS transistor, wherein the power supply voltage is applied to the source of the second PMOS transistor, the output signal output from the first sense-amplifying unit is applied to the gate of the second PMOS transistor, and the drain of the second PMOS transistor is connected to the second output node;

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the second output node, the output signal is applied to the gate of the first NMOS transistor, and the source of the first NMOS transistor is connected to the controller;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second output node, the output signal is applied to the gate of the second NMOS transistor, and the source of the second NMOS transistor is connected to the current source; and

a third NMOS transistor, wherein the drain of the third NMOS transistor is connected to the source of the first NMOS transistor, the complementary signal of the input signal is applied to

the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the controller.

61. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the controller comprises:

a first NMOS transistor, wherein the drain of the first NMOS transistor is connected to the first sense-amplifying unit, and the power supply voltage is applied to the gate of the first NMOS transistor;

a second NMOS transistor, wherein the drain of the second NMOS transistor is connected to the second sense-amplifying unit, and the ground voltage is applied to the gate of the second NMOS transistor;

a third NMOS transistor, wherein the drain of the third NMOS transistor is commonly connected to the source of the first NMOS transistor and the source of the second NMOS transistor, the reset signal is applied to the gate of the third NMOS transistor, and the source of the third NMOS transistor is connected to the current source; and

a fourth NMOS transistor, wherein the drain of the fourth NMOS transistor is commonly connected to the source of the first NMOS transistor and the source of the second NMOS transistor, the inverted signal of the reset signal is applied to the gate of the fourth NMOS

transistor, and the source of the fourth NMOS transistor is connected to the current source.

62. (New) A sense amplifier comprising:

a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal;

a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal;

a controller which is connected to the first sense-amplifying unit and the second sense-amplifying unit, resets the output signal and sets the complementary signal of the output signal in response to a reset signal and an inverted signal of the reset signal; and

a current source which is connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller and responds to the clock signal; wherein the current source includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit, the second sense-amplifying unit, and the controller, and the clock signal is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor.